What is claimed is:

1. A picture element, comprising:

a semiconductor substrate of a first conductive type having a first surface thereof;

a transistor located within the semiconductor substrate for amplifying charges;

a charge accumulation region of a second conductive type located within the semiconductor substrate, the charge accumulation region having a margin that is oriented toward the transistor;

a depletion prevention region of the first conductive type located between the charge accumulation region and the first surface of the semiconductor substrate, the depletion prevention region having a margin that is oriented toward the transistor; and

a transfer gate located on the first surface of the semiconductor substrate between the depletion prevention region and the transistor, the transfer gate controlling transfer of charges from the charge accumulation region to the transistor;

wherein said depletion prevention region margin is not closer to the transistor than said charge accumulation region margin and said charge accumulation region margin does not contact the first surface of the semiconductor substrate.

2. The picture element of claim 1, wherein the transfer gate overlaps said depletion prevention region margin and said charge accumulation region margin.

3. The picture element of claim 1 wherein the transistor is a junction field effect transistor.

4. The picture element of claim 1 wherein the transistor is a bipolar transistor.

5. The picture element of claim 1 wherein the transistor is a metal-oxide semiconductor transistor.

6. The picture element described of claim 1 wherein said charge accumulation region margin is 0.0 to 0.2 μm closer to the transistor than said depletion prevention region

margin.

7. The picture element of claim 1 wherein the transistor includes a gate of the second conductive type, a channel of the first conductive type, a deep gate of the second conductive type, a source of the first conductive type, and a drain of the first conductive type.

8. The picture element of claim 1 wherein the first conductive type is an N-type semiconductor and the second conductive type is a P-type semiconductor.

9. The picture element of claim 1 wherein the transfer gate is a metal-oxide semiconductor gate.

10. A solid picture element, comprising:

a semiconductor substrate of a first conductive type having a well of a second conductive type, and the semiconductor substrate having a first surface;

a charge accumulation layer of the first conductive type located in the well and having a first margin;

a depletion prevention layer of the second conductive type located proximate the first surface of the semiconductor substrate;

a transistor for amplifying charges; and

a transfer gate, located on the first surface of the semiconductor substrate, for controllably transferring charges from the charge accumulation layer to the transistor;

wherein no portion of the charge accumulation layer contacts the first surface of the semiconductor substrate.

11. The solid picture element of claim 10 wherein no portion of the depletion prevention layer is closer to the transistor than the first margin of the charge accumulation layer.

12. The solid picture element of claim 10 wherein the first margin of the charge accumulation layer is 0.0 to 0.2 μm closer to the transistor than any portion of the depletion prevention layer.

13. The solid picture element of claim 10 wherein the transfer gate overlaps the

first margin of the charge accumulation layer.

14. The solid picture element of claim 10 wherein the transfer gate is a metal-oxide semiconductor gate.

15. The solid picture element of claim 10 wherein the transistor is a junction field effect transistor.

16. The solid picture element of claim 10 wherein the transistor is a bipolar transistor.

17. The solid picture element of claim 10 wherein the transistor is a metal-oxide semiconductor transistor.

18. A method of transferring a charge from a charge accumulation layer to a transistor of a solid picture element so as to substantially eliminate residual images, comprising the steps:

locating a charge accumulation region of a first conductive type within a semiconductor substrate having a first surface such that no portion of the charge accumulation region contacts the first surface of the semiconductor substrate;

locating a depletion prevention region within the semiconductor substrate between the charge accumulation region and the first surface;

locating a transfer gate on the first surface of the semiconductor substrate such that the transfer gate overlaps a portion of the charge accumulation region; and

locating a transistor within the semiconductor substrate, the transistor being in communication with the transfer gate for receiving a charge from the charge accumulation region and amplifying the charge.

19. The method of claim 18 further comprising the step of locating the charge accumulation region so as to orient a first margin of the charge accumulation region toward the transistor and locating the depletion prevention region so that no portion of the depletion prevention region is closer to the transistor than the first margin of the charge accumulation region.

20. The method of claim 18 further comprising the step locating a first margin of

the charge accumulation region 0.0 to 0.2 μm closer to the transistor than any portion of the depletion prevention region.

21. The method of claim 18 wherein the transistor is a field effect transistor.

22. The method of claim 18 wherein the transistor is a bipolar transistor.

23. The method of claim 18 wherein the transistor is a metal-oxide semiconductor transistor.

24. The method of claim 18 wherein the transfer gate is a metal-oxide semiconductor gate.

25. A method of manufacturing a solid picture element having a semiconductor substrate of a first conductive type with a well of a second conductive type, a transistor for amplifying charges, a charge accumulation region of the first conductive type located within the semiconductor substrate and having a margin located a first distance from the transistor, a depletion prevention region of the second conductive type located between the charge accumulation region and an upper surface of the semiconductor substrate and having a margin located a second distance from the transistor, and a transfer gate coupled to the upper surface of the semiconductor substrate overlapping a portion of the depletion prevention region and the transistor, comprising the steps:

implanting ions of the first conductive type at a first angle to the upper surface of the semiconductor substrate using the transfer gate as a mask and forming the charge accumulation region such that it is within the semiconductor substrate and does not contact the upper surface of the semiconductor substrate; and

implanting ions of the second conductive type at a second angle to the upper surface of the semiconductor substrate using the transfer gate as a mask and forming the depletion prevention region such that it is between the charge accumulation region and the upper surface of the semiconductor substrate;

wherein the first angle is not greater than the second angle thereby causing the first distance of the charge accumulation region margin to the transistor to be no greater than the second distance of the depletion prevention region margin to the transistor.

26. The method of claim 25 wherein the first angle is between 30 degrees and 80 degrees and the second angle is substantially 90 degrees.

27. The method of claim 25 wherein the first angle is between 40 degrees and 60 degrees and the second angle is substantially 90 degrees.

28. The method of claim 25 wherein the first angle is between 30 degrees and 80 degrees and the second angle is between 80 degrees and 90 degrees.

29. The method of claim 25 wherein the first angle and the second angle are substantially equal and the charge accumulation region margin and the depletion prevention region margin are substantially the same distance from the transistor.

30. The method of claim 25 wherein the second distance from the transistor to the depletion prevention region margin is between 0.0 and 0.2 μm greater than the first distance from the transistor to the charge accumulation region margin.

31. A method of manufacturing a solid picture element having a semiconductor substrate of a first conductive type with a well of a second conductive type, a transistor for amplifying charges, a charge accumulation region of the first conductive type located within the semiconductor substrate and having a margin located a first distance from the transistor, a depletion prevention region of the second conductive type located between the charge accumulation region and an upper surface of the semiconductor substrate and having a margin located a second distance from the transistor, and a transfer gate coupled to the upper surface of the semiconductor substrate overlapping a portion of the depletion prevention region and the transistor, comprising the steps:

implanting ions of the first conductive type into the semiconductor substrate using the transfer gate as a mask and forming the charge accumulation region such that it is within the semiconductor substrate and does not contact the upper surface of the semiconductor substrate;

locating an oxide film on the transfer gate thereby increasing the footprint of the transfer gate on the upper surface of the semiconductor substrate; and

implanting ions of the second conductive type into the semiconductor substrate using the transfer gate with oxide film as a mask and forming the depletion prevention region such that it is between the charge accumulation

region and the upper surface of the semiconductor substrate, and the first distance of the charge accumulation region margin to the transistor is not greater than the second distance of the depletion prevention region margin to the transistor.

32. The method of claim 31 further comprising the step of selecting a thickness of the oxide film so that the second distance is not more than 0.2 μm greater than the first distance.

33. The method of claim 31 further comprising the step of selecting a thickness of the oxide film so that the first distance approximately 0.1 μm less than the second distance.

34. A method of manufacturing a solid picture element having a semiconductor substrate of a first conductive type with a well of a second conductive type, a transistor for amplifying charges, a charge accumulation region of the first conductive type located within the semiconductor substrate and having a margin located a first distance from the transistor, a depletion prevention region of the second conductive type located between the charge accumulation region and an upper surface of the semiconductor substrate and having a margin located a second distance from the transistor, and a transfer gate coupled to the upper surface of the semiconductor substrate overlapping a portion of the depletion prevention region and the transistor, comprising the steps:

implanting ions of the first conductive type into the semiconductor substrate using the transfer gate as a mask and forming the charge accumulation region such that it is within the semiconductor substrate and does not contact the upper surface of the semiconductor substrate;

locating and etching an insulating film on an end wall of the transfer gate; and

implanting ions of the second conductive type into the semiconductor substrate using the insulating film as a mask and forming the depletion prevention region such that it is between the charge accumulation region and the upper surface of the semiconductor substrate, and the first distance of the charge accumulation region margin to the transistor is not greater than the second distance of the depletion prevention region margin to the transistor.

35. The method of claim 34 further comprising the step of locating and etching the insulation film so that the first distance is not less then 0.2 μm of the second distance.

36. The method of claim 34 further comprising the step of implanting the ions of the second conductive type at an angle to the upper surface.

37. The method of claim 34 further comprising the step of implantation the ions of the second conductive type at an angle to the upper surface of between 80 degrees and 90 degrees.

38. A method of manufacturing a solid picture element having a semiconductor substrate of a first conductive type with a well of a second conductive type, a transistor for amplifying charges, a charge accumulation region of the first conductive type located within the semiconductor substrate and having a margin located a first distance from the transistor, a depletion prevention region of the second conductive type located between the charge accumulation region and an upper surface of the semiconductor substrate and having a margin located a second distance from the transistor, and a transfer gate coupled to the upper surface of the semiconductor substrate for transferring charges from the charge accumulation region to the transistor, the method comprising the steps:

forming a mask layer on the semiconductor substrate, the mask layer having a mask margin located a third distance from the transistor;

implanting ions of the first conductive type into the semiconductor substrate using the mask layer as a mask and forming the charge accumulation region such that the charge accumulation region is within the semiconductor substrate and does not contact the upper surface of the semiconductor substrate;

removing the mask layer;

forming the transfer gate on top of the semiconductor substrate and locating an end margin of the transfer gate such that the end margin is located a fourth distance from the transistor and the fourth distance is greater than the third distance of the mask margin from the transistor; and

implanting ions of the second conductive type into the semiconductor substrate using the transfer gate as a mask and forming the depletion prevention region such that it is between the charge accumulation region and the upper surface of the semiconductor substrate and the first distance of the charge accumulation region margin to the transistor is less than the second

distance of the depletion prevention region margin to the transistor.

39. The method of claim 38 wherein the third distance and the fourth distance are selected such that the first distance is not less than the second distance by more than 0.2 μm.